<div align="center">REMARKS/ARGUMENTS</div>

By this paper, Applicant responds to the Office Action of October 28, 2005 and respectfully requests reconsideration of the application. A Petition for Extension of Time extends the time for response through March 28, 2006. Accordingly, this response is timely.

Claims 1, 3-6, 8, 9, and 12-58 are now pending, a total of 54 claims. Claims 1, 5, 13, 14, 20, 23, 30, 35, 41, 44, 49 and 55 are independent. Claims 1 and 14-53 are allowed, and 3 and 4 are indicated to recite allowable subject matter.

I.   Claim 5

Claim 5 is compared to certain portions of Colwell '728, Papworth '473 and Hammond '525 in ¶¶ 1-6 of the Office Action. Claim 5 recites as follows:

> 5. A method comprising the steps of:
>
> decoding a macroinstruction of a computer, the decoding of the macroinstruction generating a plurality of iterations of:
>
>> a pattern of microinstructions implementing a basic operation, wherein **the microinstruction set is architecturally exposed** to programs fetched from an architecturally-visible memory of the computer, and
>>
>> a branch instruction predicted not taken.

Claim 5 recites that the "microinstruction set is architecturally exposed." This language is discussed in ¶¶ 5 and 6 of the Office Action.

A.   The Office Action Mischaracterizes Colwell '728

The first sentence of paragraph 5 of the Office Action reads "As per claim 5 Colwell taught that microinstruction set architecturally available ..." and points to col. 12, lines 19-20. The Office Action is not correct. Colwell '728 col. 12, lines 19-20 states exactly opposite the characterization in the Office Action:

> For micro branch instructions, the prediction bit may be set by a (human) microcode programmer...

If the "prediction bit" may only be set by a "microcode programmer" then the micro instruction is not "architecturally exposed" as that term is understood by those of ordinary skill (in the

conventional relationship between microcode and architectural code discussed in Colwell '728). See Response of 9/27/05 at § IV(A)(1), at pages 15-17.

The very portion cited by the Office Action demonstrates that Colwell's microcode is not "architecturally exposed." Because claim 5 recites a limitation that is absent from the art, claim 5 cannot be obvious.

B.   The Office Action Is Procedurally Incomplete and Raises No Rejection

Claim 5 recites "microinstruction set is architecturally exposed to programs fetched from an <u>architecturally-visible memory</u>. For two separate reasons, the Office Action is procedurally inadequate to raise any rejection whatsoever.

First, the Office Action does not address the language of claim 5. The closest discussion of this claim language appears to be paragraph 5, which simply discusses a "memory," not an "<u>architecturally-visible memory</u>."

Second, the argument made in § I.A has been put before the Examiner twice before, Response of 9/27/05 at § IV(A)(1), at pages 15-17; Response of May 13, 2005 at 13-14. This Office Action is simply silent in reply. It fails to "answer all material traversed" as required by MPEP § 707.07(f).

If any rejection is raised in the next Office Action, Applicant respectfully observes that it will be a "new ground of rejection."

C.   Colwell '728 Is Unavailable as an Obviousness Reference vis-à-vis Claim 5

Colwell '728 is not available as a reference against claim 5. The following legal principles from MPEP § 2143.01 apply (quotations and citations omitted):

V.   THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE

If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, <u>then there is no suggestion or motivation to make the proposed modification</u>. ... The court reversed, finding that if the prior art device was turned upside down it would be inoperable for its intended purpose because the gasoline to be filtered would be trapped at the top, the water and heavier oils sought to be separated would flow out of the outlet instead of the purified gasoline, and the screen would become clogged..

...

VI. THE PROPOSED MODIFICATION CANNOT CHANGE THE PRINCIPLE OF OPERATION OF A REFERENCE

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.

Colwell '728 is directed to conventional commercial Intel X86 processors. Colwell '728 col. 4, lines 60-62; col. 7, lines 17-18. As discussed in Exhibit A, the "principle of operation" of microcode in general-purpose commercial processors is to keep the details of a computer's microarchitecture hidden from users for at least three reasons: (a) portability: to separate "the nitty gritty details of a particular machines' design" hidden so that "programs written for a particular ISA [instruction set architecture] could now run on any machine that implemented that ISA", (b) reliability: exposing the i486 microarchitecture would compromise system reliability, and (c) simplicity: the interactions between i486 microinstructions are extremely complex, and must be managed by special hardware, not by programmers.

The modification of Colwell '728 proposed in the Office Action – architecturally exposing the i486 microcode – would violate the "principle of operation" of microcode as used in Colwell '728. It would also render Colwell '728 "unsuitable for its intended purpose," a general purpose commercial microprocessor with an architecture that remains consistent from generation to generation, while the microengine can change.

Colwell '728 may not be modified as proposed in the Office Action. Colwell '728 may not be used as a reference, alone or in combination, against claim 5.

Papworth '473 likewise appears to be directed to conventional general-purpose microprocessors such as the Intel X86 (note the references throughout to X86 register names), and likewise may not be applied against claim 5 without violating MPEP § 2143.01.

D.   Call for Evidence Pursuant to 37 C.F.R. § 1.104(d)(2)

A number of statements in the Office Action lack evidentiary support. Pursuant to 37 C.F.R. § 1.104(d)(2), Applicant requests a reference or affidavit to support each of the following statements:

- That designers of conventional general-purpose commercial processors, as discussed in Colwell '728, would have considered it desirable to "allow the user or programmer in the Colwell system [or] Papworth system to directly use microinstructions." Office Action ¶ 17. As is well know to those of ordinary skill, and noted in Exhibit A, this would be disastrous in Colwell's or Papworth's general-purpose commercial product.

- That it was recognized to be desirable to "allow[ ] additional flexibility to the programmer or user in the implementation of the combined system to tailor or fine tune or optimize applications." Office Action ¶ 17. One crucial purpose of the Intel architecture discussed in Colwell and Papworth is to prevent a programmer or user from doing things that ought not be done.

The Office Action correctly points out a number of advantages of the invention, and a number of problems that had to be solved to make it work. However, the Office Action points to nothing in the prior art that recognized that these advantages were known or predicted, or that the solutions were known. The positions stated in the Office Action appear to be hindsight gained from the application.

If any rejection is maintained, Applicant respectfully requests – pursuant to 37 C.F.R. § 1.104(d)(2) – substantial evidence showing that the advantage or motivation was known in the art, and was known to be consistent with general purpose, multi-generation microprocessors like the Intel X86 family.

E.   The Office Action is Silent on Reasonable Expectation of Success

MPEP §§ 2142, 2143, and 2143.02 requires that an Office Action make a showing of "reasonable expectation of success." The Office Action is silent on this issue. The Office Action is procedurally too incomplete to raise any multi-reference rejection.

The Office Action makes no showing that, for example, Hammond's RISC instruction set could be used as a microcode instruction set for implementing Colwell's 80486, or that Colwell's 486 microcode could be architecturally exposed for use in Hammond's system. There are a number of issues that would make either such combination essentially unworkable, however, until an Office Action sets forth a *prima facie* case, the problems are too numerous to discuss.

F.   Conclusion: Claim 5 is Not Rejected, and Is Patentable on the Merits

For all these reasons, the Office Action is procedurally inadequate to raise any rejection of claim 5. Further, claim 5 is patentable on the merits.

II.   Claim 55

Claim 55 is added in this Response and recites as follows.

> 55.   A computer, comprising:
>
> an instruction decoder designed to decode macroinstructions into microinstructions for execution in an instruction pipeline on a computer, and for at least one macroinstruction, the decoder being designed to generate a plurality of iterations of a pattern of microinstructions implementing a basic operation of the macroinstruction, **a microinstruction of each of the plurality of iteration patterns carrying a marker indicating that the marked microinstruction defines a boundary between two successive iterations**, the microinstruction set being architecturally exposed for execution from an architecturally-exposed memory; and
>
> operand commit circuitry designed to detect the marker, and in response, to commit results of an iteration to architectural state of the computer.

Claim 55 recites that "a plurality" of microinstructions generated from a single macroinstruction each carry "a marker indicating that the marked microinstruction defines a boundary between successive iterations." That is, "a plurality of" microinstructions generated from a single macroinstruction carry the marker. Claim 55 also recites operand commit circuitry responsive to the marker that commits iteration results to architectural state.[1]

Claim 55 distinguishes the "beginning of macro instruction" and "end of macro instruction" flow markers of Colwell '728.[2] Colwell '728 explains that he must provide exactly one beginning marker, and exactly one end marker per instruction, because certain actions – such as updating the IP, enabling and disabling interrupts, committing intermediate results to architecturally-visible state, etc. – must occur exactly once per macroinstruction. *E.g.*, Colwell '728, col. 24, line 11, col. 25, line 5, col. 25, lines 35-37. If iteration results were held to the end of the instruction, as might occur with Colwell's markers, or Colwell's end-of-instruction processing occurred in the middle of an instruction, the computer would execute incorrectly.

Neither Colwell '728 nor Papworth '473 are available as obviousness references against claim 55, because the claim would "render the prior art unsatisfactory for its intended purpose" and "change the principle of operation of a reference".

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[1] This is one of the exceptions to the general rule that "architectural state" is the state that is visible at instruction boundaries.

[2] Note that claim 56 makes absolutely clear that any "end of macroinstruction" marker is different than the "iteration boundary" marker of claim 55.

For these reasons, claim 55 distinguishes Colwell '728 and any combination involving either Colwell '728 or Papworth '473.

III. Claim 13

Claim 13 is compared to certain portions of Colwell '728 and Papworth '473 in ¶¶ 9-14 of the Office Action. Claim 13 recites as follows:

> 13. A computer, comprising:
> an instruction decoder designed to decode macroinstructions into microinstructions for execution in an instruction pipeline on a computer, and for at least one macroinstruction, the decoding of the macroinstruction generating a plurality of iterations of:
>> a pattern of microinstructions implementing a basic operation, and
>> a branch microinstruction predicted not taken, wherein the branch microinstruction is generated **carrying a marker indicating that the branch microinstruction defines a boundary between two successive iterations;**
> the instruction decoder being further designed to cease generating iterations on detection of a branch mispredict.

A. The Office Action Misparaphrases the Claim

In ¶ 14, the Action discusses a microinstruction that defines a "boundary." But claim 13 does not recite a "boundary." It recites a plurality of microinstructions, each with a marker indicating "**a boundary <u>between two successive iterations</u>**" within a <u>single</u> macroinstruction.

Because the Office Action does not address the claim language, it is procedurally incomplete, and inadequate to raise any rejection whatsoever. Applicant respectfully requests that the claim be treated as a whole. Applicant also notes that any future rejection of claim 13 will necessarily be a "new ground of rejection" that prevents final rejection.

B. The Modification of the Prior Art Hinted in the Office Action Would Render the Prior Art Unsatisfactory for its Intended Purpose

Though the Office Action does not set out any position clearly or completely enough to allow a direct response, in an effort to advance prosecution, Applicant observes as follows. MPEP § 2143.01 instructs as follows:

2143.01 Suggestion or Motivation To Modify the References
THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART
UNSATISFACTORY FOR ITS INTENDED PURPOSE
If proposed modification would render the prior art invention being
modified unsatisfactory for its intended purpose, then there is no
suggestion or motivation to make the proposed modification. *In re Gordon*,
733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) (... The Board concluded
the claims were prima facie obvious, reasoning that it would have been
obvious to turn the reference device upside down. The court reversed,
finding that if the prior art device was turned upside down it would be
inoperable for its intended purpose...).

Perhaps the Office Action is hinting that it is thought obvious to mark "a plurality of"

microinstructions generated within a single macroinstruction with Colwell's "beginning of macro

instruction" and "end of macro instruction" markers.

If either of Colwell's flow markers were applied to "a plurality of" microinstructions

within a single macroinstruction, as recited in claim 13, the hypothetical combined computer

would break. Colwell's "beginning of macro instruction" and "end of macro instruction" are

used to indicate actions that must occur only once per macroinstruction, and must occur only on

instruction boundaries, such as updating the IP, allowing interrupts, architecturally committing

intermediate state, etc. (*e.g.*, Colwell '728 col. 24, line 11, col. 25, line 5, col. 25, lines 35-37). If

those actions were taken at "iteration boundaries" while an instruction is in progress, then those

actions would be performed at the wrong time and the wrong number of times. The hypothetical

computer proposed in the Office Action would malfunction.

The Office Action asserts that modification "would have provided a boundary between

iterations." The Office Action cites no evidence to suggest that this problem was known, that

any solution was desirable, or that the particular marker recited in claim 13 was a known

solution. If it is maintained that this modification is obvious, Applicant requests a reference or

affidavit, pursuant to 37 C.F.R. § 1.104(d)(2), showing that the motivation, the problem and the

solution were known in the art.

Applicant notes that this argument is copied almost verbatim from the previous paper.

The October 2005 Office Action fails to "answer all material traversed" as required by MPEP

§ 707.07(f). Prosecution cannot progress when an Examiner is silent. If any rejection is raised

in the next Office Action, Applicant respectfully observes that it will be a "new ground of rejection."

IV.   Dependent Claims

Dependent claims 12 are patentable with the independent claims discussed above. In addition, the dependent claims recite additional features that further distinguish the art.

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. A Petition for Extension of Time for two months is set forth above. In the event that further extension of time is required, Applicant petitions for that extension of time required to make this response timely. Kindly charge any additional fee, or credit any surplus, to Deposit Account No. 23-2405, Order No. 114596-31-000127BS.

Respectfully submitted,

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Dated: <u>March 28, 2006</u>   By: _____

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